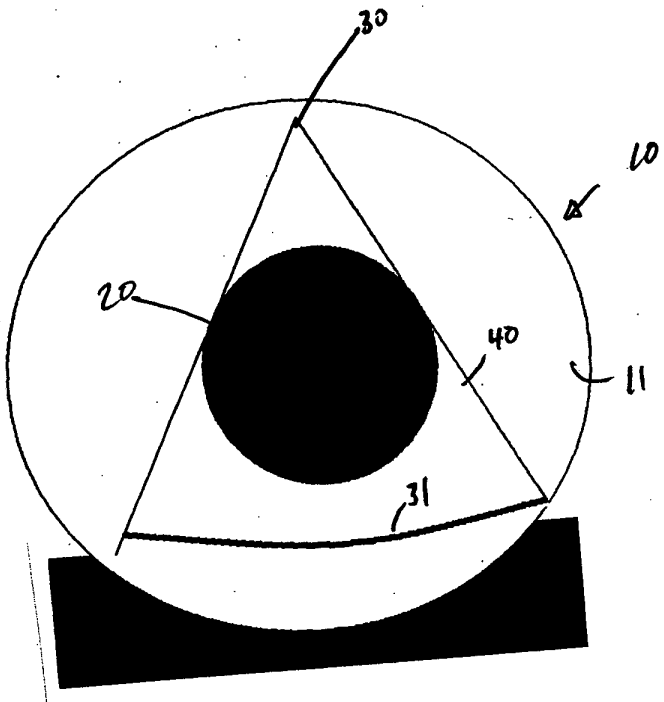


FIG. 1

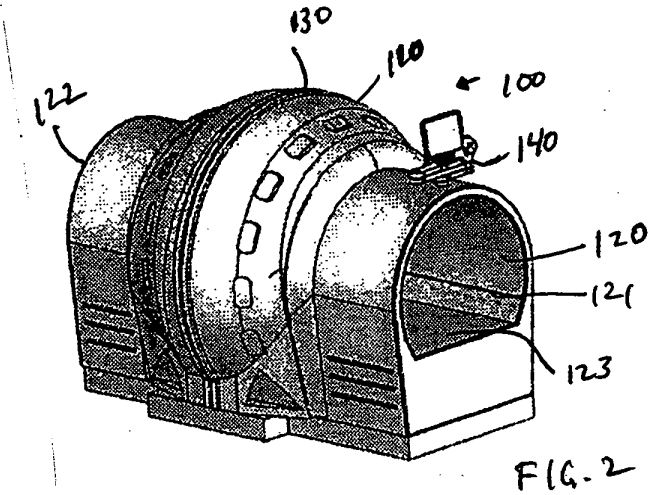


FIG. 2

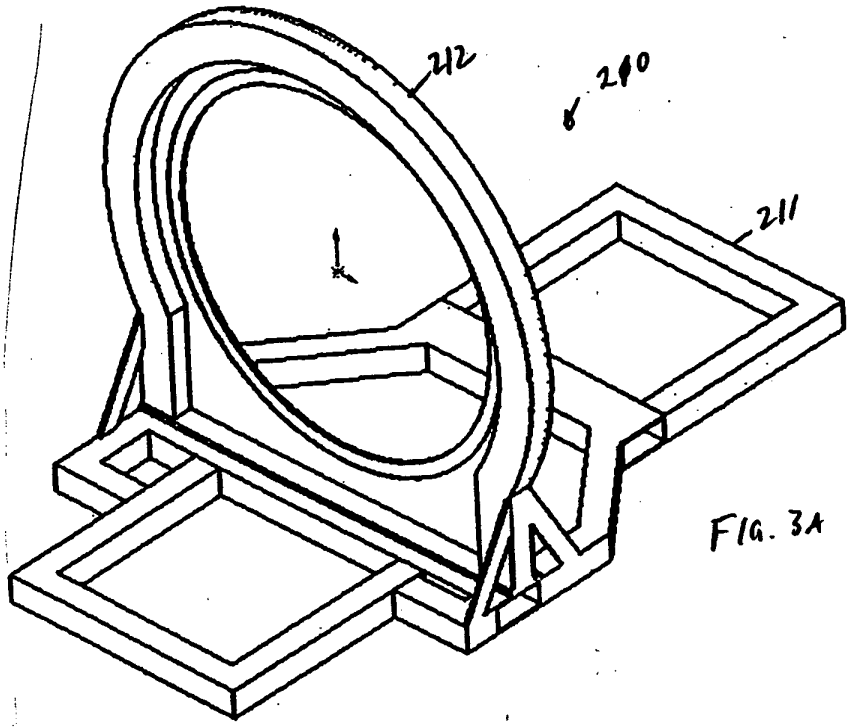


FIG. 3A

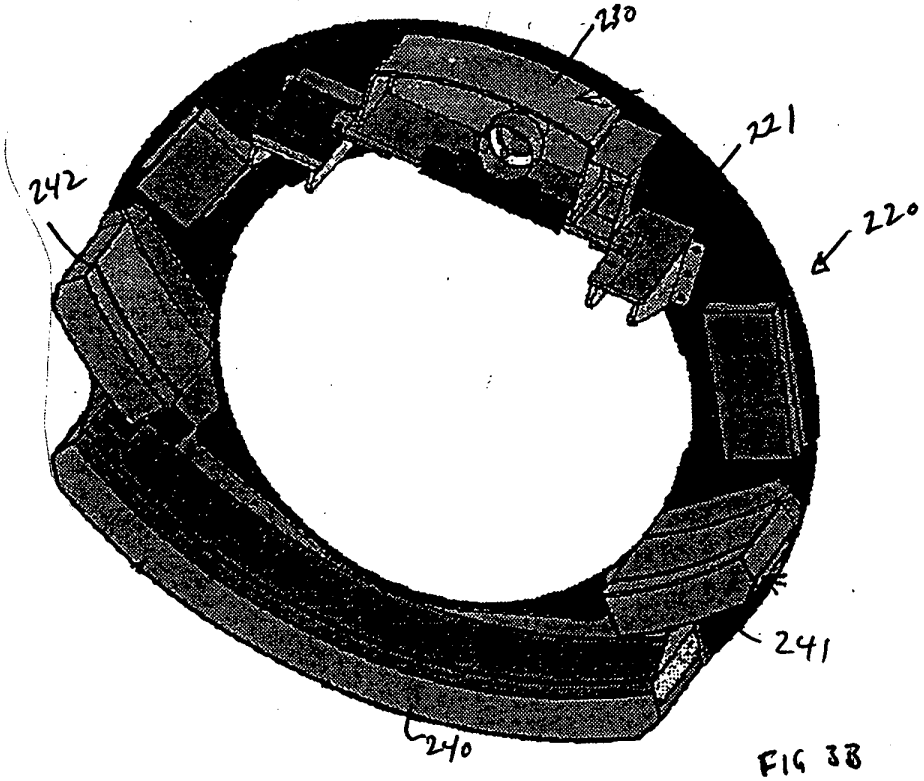


FIG 3B

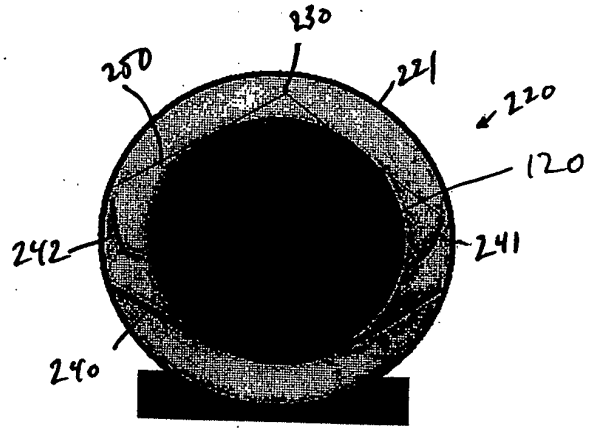


FIG. 4

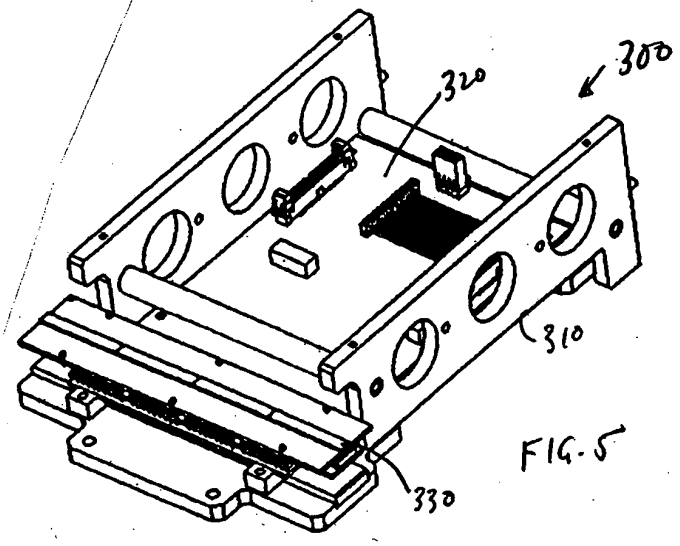


FIG. 5

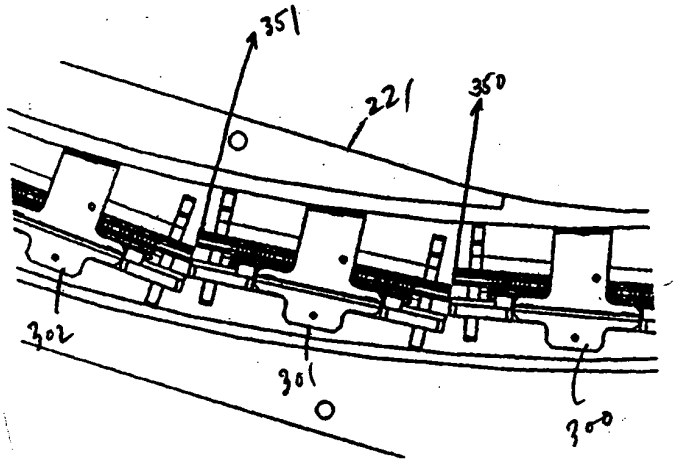


FIG. 6

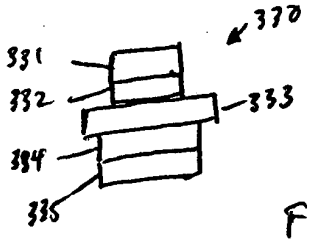


FIG 7

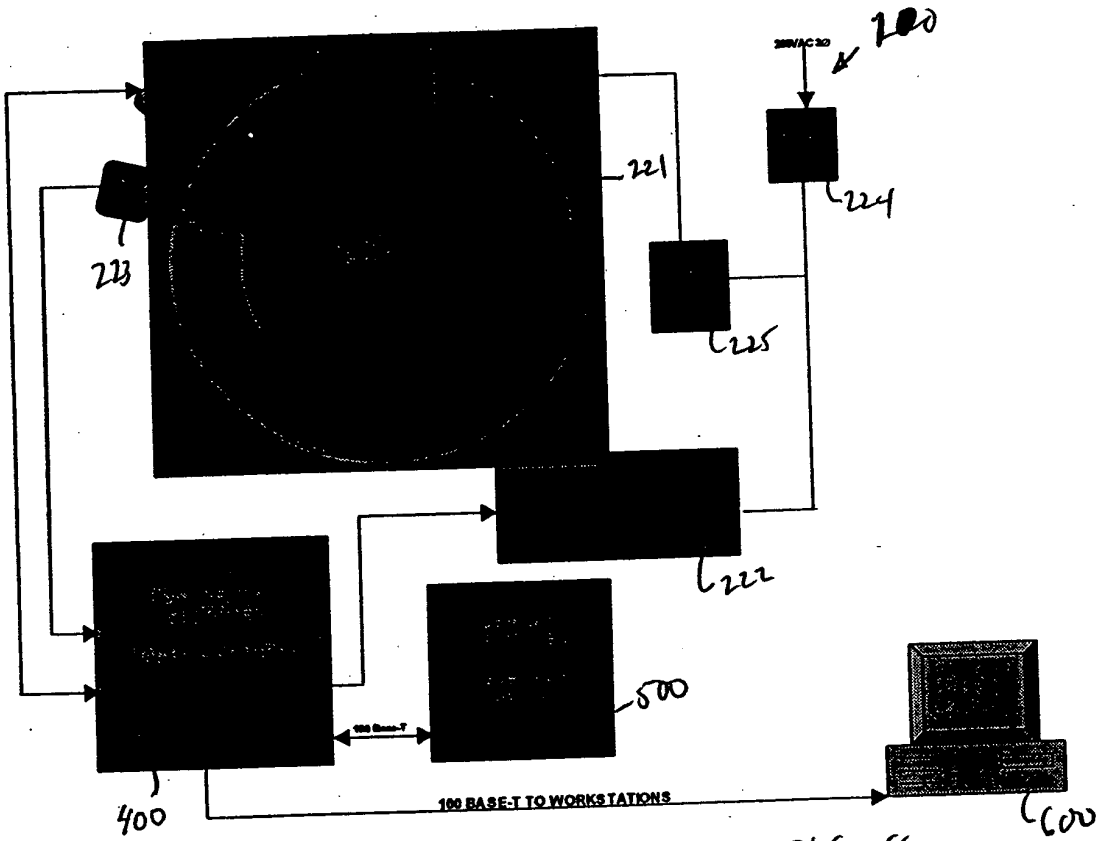


FIG. 8

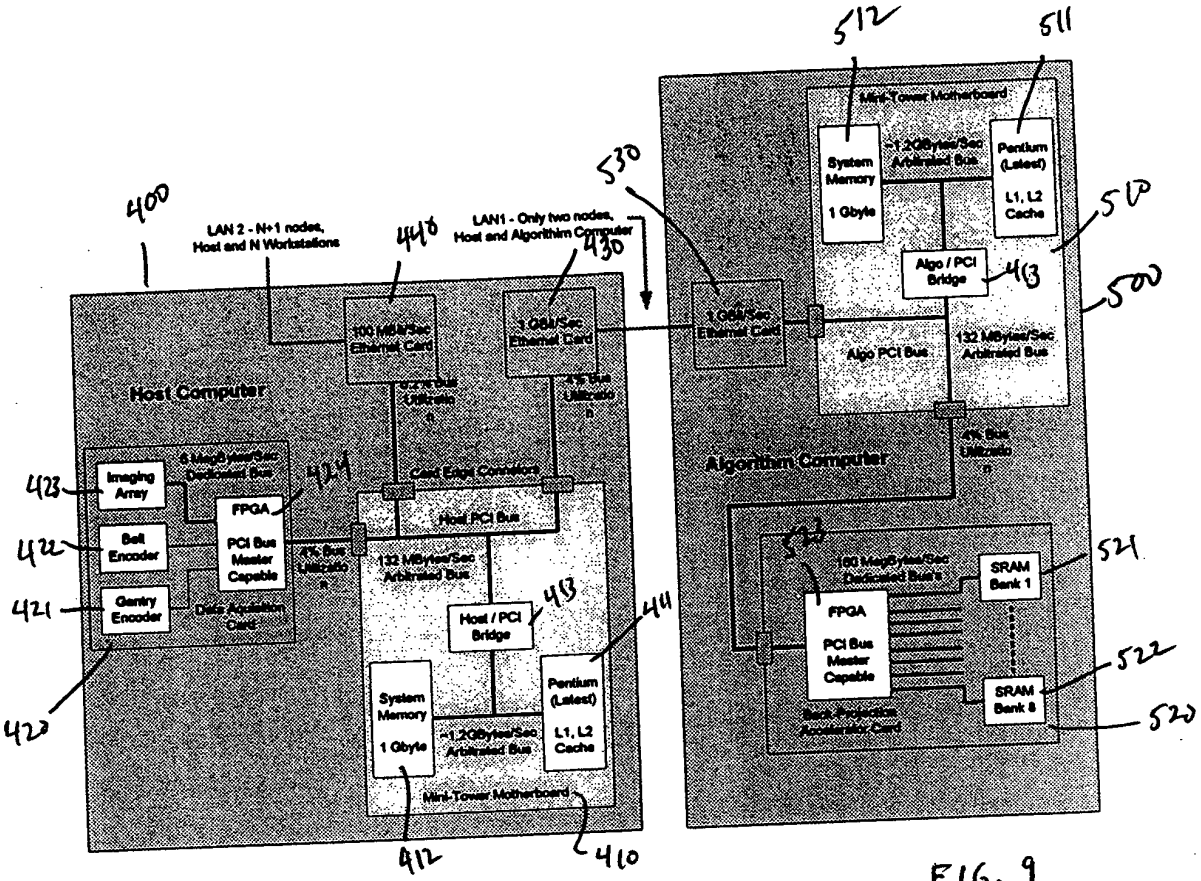

400
LAN 2 - N+1 nodes, Host and N Workstations
440
LAN1 - Only two nodes, Host and Algorithm Computer
430
530
512
511
Mini-Tower Motherboard
System Memory
1 Gbyte
~1.2GBytes/Sec Arbitrated Bus
Pentium (Latest)
L1, L2 Cache
517
Algo / PCI Bridge
513
500
1 GB/Sec Ethernet Card
Algo PCI Bus
132 MBytes/Sec Arbitrated Bus
4% Bus Utilizatio n
Algorithm Computer
100 MBit/Sec Ethernet Card
1 GBit/Sec Ethernet Card
Host Computer
Card Edge Connectors
Host PCI Bus
Imaging Array
6 MegaBytes/Sec Dedicated Bus
423
424
FPGA
PCI Bus Master Capable
Belt Encoder
422
Gantry Encoder
421
Data Acquisition Card
4% Bus Utilizatio n
132 MBytes/Sec Arbitrated Bus
Host / PCI Bridge
413
414
System Memory
1 Gbyte
~1.2GBytes/Sec Arbitrated Bus
Pentium (Latest)
L1, L2 Cache
Mini-Tower Motherboard
420
412
410
520
100 MegaBytes/Sec Dedicated Bus's
FPGA
PCI Bus Master Capable
Back-Projection Accelerator Card
SRAM Bank 1
SRAM Bank 8
524
522
520

FIG. 9

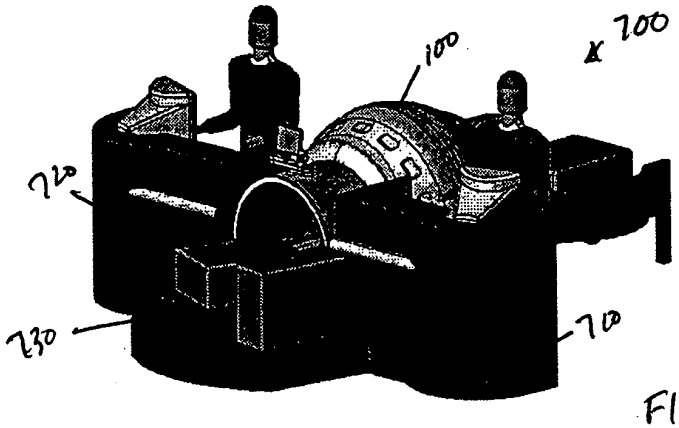
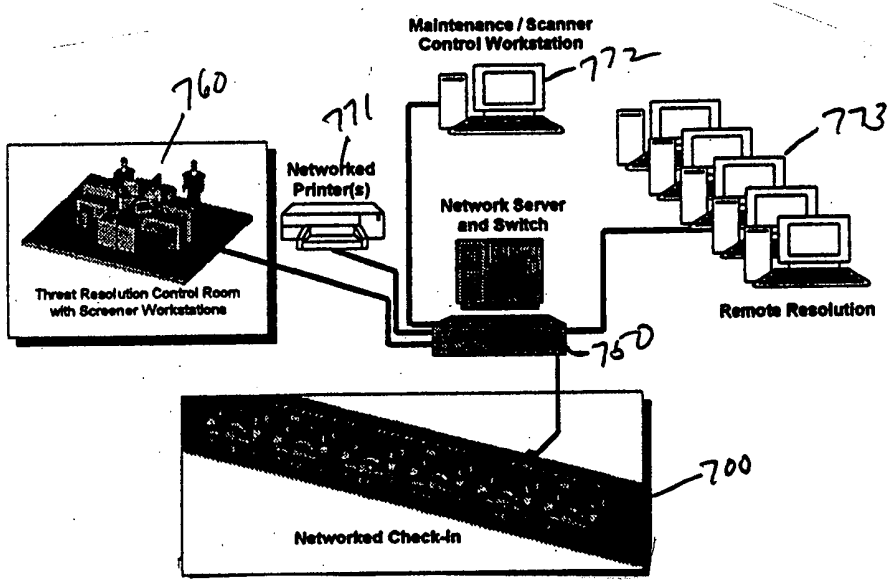

100
700
720
730
710

FIG. 10

FIG 11


Maintenance / Scanner Control Workstation
772
760
771
773
Networked Printer(s)
Network Server and Switch
Threat Resolution Control Room with Screener Workstations
Remote Resolution
750
700
Networked Check-In

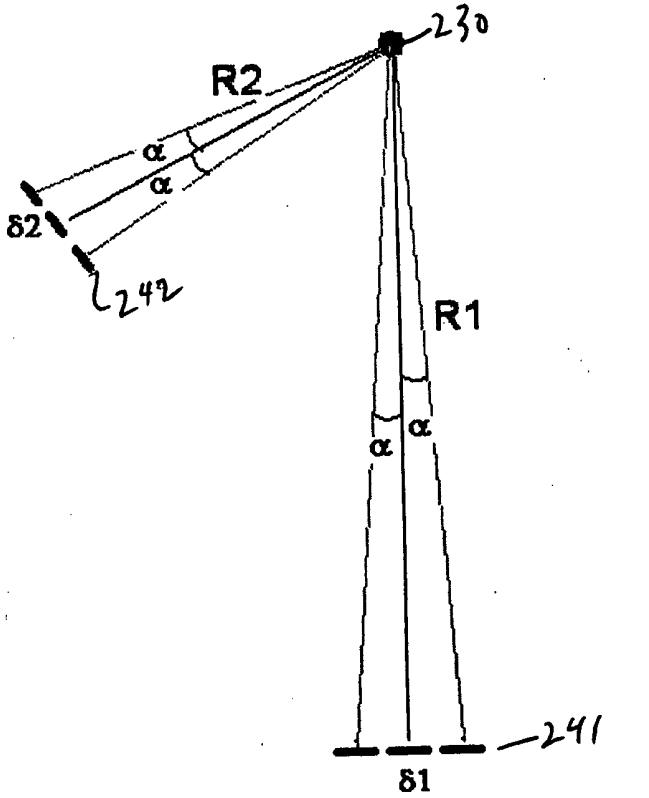

230
R2
α
α
δ2
242
R1
α
α
241
δ1

FIG 12

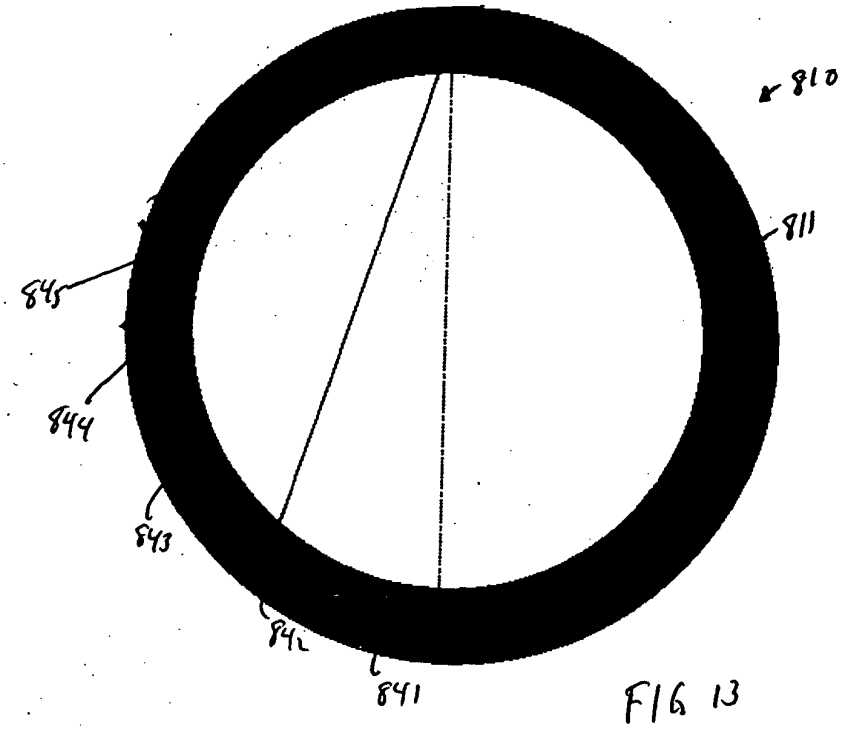

810
811
845
844
843
842
841

FIG 13

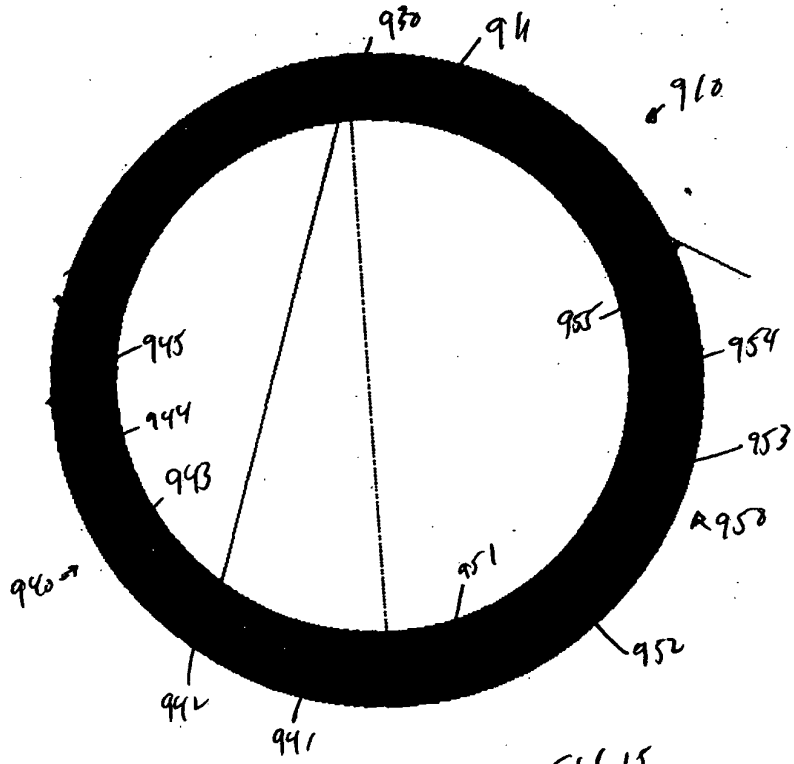

930
94
910
945
944
943
955
954
953
950
940
951
952
942
941

FIG. 15

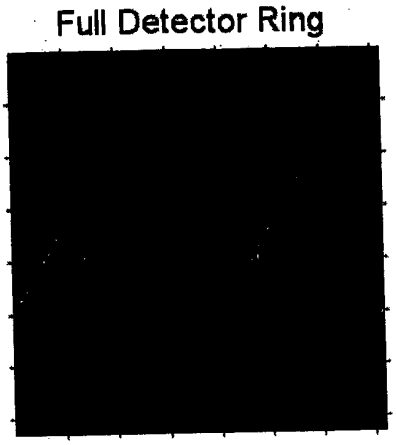


FIG. 14A

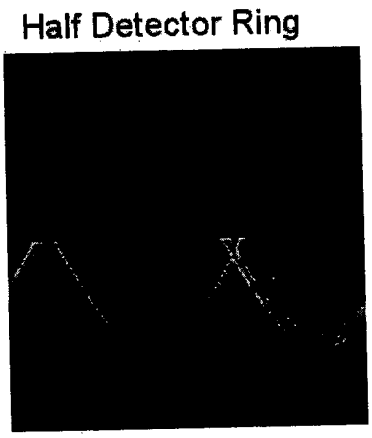


FIG. 14B

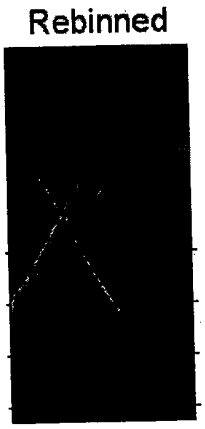


FIG. 14C